An Improved Multipeak Resonant Tunneling Diode Model for Nine-State Resonant Tunneling Diode Memory Circuit Simulation

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***Abstract*— A simple SPice equivalent circuit model for simulating current-voltage (I-V) characteristics and logic operation waveforms of eight-peak resonant tunneling diode exhibits the simulated results agreed well with experimental data measured from an eight-peak resonant tunneling diode device fabricated at Seabaugh's experiment, which we show through PSpice simulation.**

I. Introduction

Multipeak resonant tunneling diodes (RTD's) have been used in various applications such as in multivalued logic (MVL) and multivalued memory (MVM) circuits. Multistable memory systems with three to nine states of RTD-based MVM circuits have been reported [1]–[7]. Among these multipeak RTD devices, an eight-peak RTD, as suggested from the experimental evidence by Seabaugh *et al.* [7] demonstrated the most large number current peaks in the RTD fabrication arena. To analyze the current-voltage (I-V) characteristics and its nine-state multistable memory performances of such high-order RTD, we developed an eight-peak RTD SPice equivalent circuit model from a new approach of modeling multipeak RTD current-voltage (I-V) characteristics [8], and implemented in PSpice run on a personal computer. The simulated results agree well with the measured current-voltage (I-V) data from [7], and obtain the expected nine-state logic levels.

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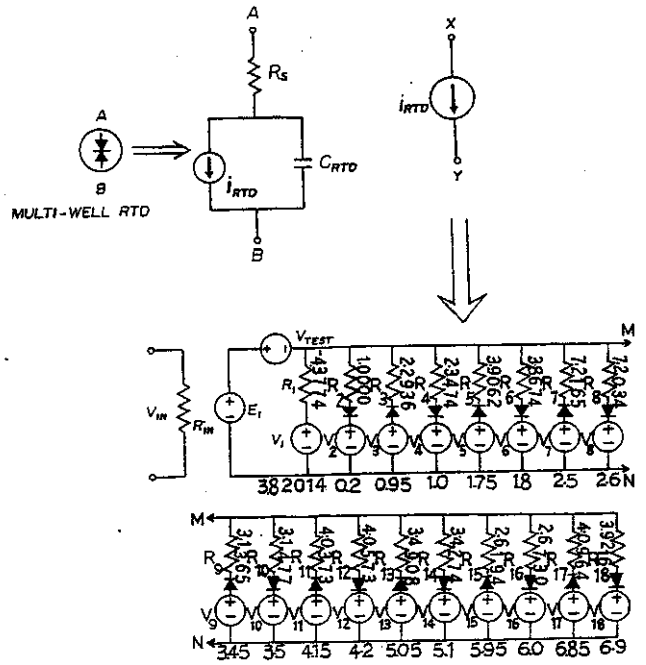

Fig. 1. An eight-peak RTD piecewise linear (PWL) I-V characteristics equivalent circuit model.

II. Model and Circuit Simulation Development

A. The Piecewise Linear (PWL) Equivalent Circuit Model of Eight-Peak RTD Current-Voltage (I-V) Characteristics

The schematic illustration of the voltage controlled current source $i_{\mathrm{RTD}}\ (\nu)$ using the piecewise linear (PWL) approximation technique for simulating the current-voltage (I-V) characteristics of eight-peak RTD is derived from [8] and depicted in Fig. 1. A dummy voltage source V_{TEST} measures the total current flowing between the parallel branches R_1V_1, and multiple sections $R_2D_2V_2\cdots R_{18}D_{18}V_{18}$. This current can be considered as the output current of the RTD or the value of voltage controlled current iRTD (ν), and form the RTD eight current peaks. The element values of R_1 and V_1 can be obtained by solving two equations simultaneously, which are derived by using Kirchhoff's voltage law (KVL) and Kirchhoff's current law (KCL), with the chosen breakpoint voltage $(V_2, V_3\cdots V_{18})$ and current values of the eight-peak RTD I-V curve inserted into the whole PWL equivalent circuit of Fig. 1. $R_2, R_3\cdots R_{18}$ can be calculated from the piecewise approximation technique [9] with the following equations (1) and (2)

$$R_n = \frac{1}{M_B - M_A} \tag{1}$$

where M_B and M_A are the slopes of two adjacent upward linear segments of the RTD I-V curve with $M_B > M_A$.

$$R_m = \frac{1}{M_C - M_D} \tag{2}$$

where M_C and M_D are the slopes of two adjacent downward linear segments of the RTD I-V curve with $M_C > M_D$. The simulated eight-peak RTD current-voltage (I-V) curve can be seen in the Fig. 2 which shows strong similarity as in Ref. [7].

B. Circuit Simulation of MESFET Depletion Load Line and Nine Logic Stable States

A nine-state RTD-based MVM circuit is simulated using PSpice run on a personal computer. The schematic model of the nine-state memory cell is referred to Fig. 2 of [8] except an extra dummy voltage source V_{TEST1} is connected between the voltage source V_{DD} and the MESFET depletion load. The maximum MESFET drain current is chosen to be midway between the RTD peak and valley currents i.e. ~1.25 mA calculated from (3) shown as follows

$$I_{\mathrm{DS}} = \beta(1 + \lambda V_{\mathrm{DS}})(V_{\mathrm{GS}} - V_{TO})^2 \tanh(\alpha V_{\mathrm{DS}}) \qquad (3)$$

where I_{DS} is the drain-to-source current, β is the quadratic transfer parameter, λ is the channel length modulation coefficient, V_{DS} is the drain-source voltage, V_{GS} is the gate-source voltage, V_{TO} is the SPice notation for pinch-off voltage, and α is a model parameter merging the linear and saturation regions and needs to be extracted from measurement. The dummy voltage source V_{TEST1} then measures the current flowing through the MESFET depletion load, and the simulated result of constant current load line are also plotted in Fig. 2 which agrees well with the measured experimental result in [7]. We next proceed to simulate the nine stable-state of this MVM circuit. By using two typical NPN transistor devices as the switch model, we can control the write and read times with the input of write and read pulse signals, $C_P(W)$ and $C_P(R)$, respectively [8]. We have deliberately chosen the timing of $C_P(W)$ and $C_P(R)$ to promise the write and read pulse signals can properly alternately turn the two NPN transistors on and off, and obtain the correct corresponding output waveforms, by using SPice statement [10]

$V(W)\quad N_+\quad N_-$

pulse(0 V_{DD} TD_W TR_W TF_W PW_W PER_W)

$V(R) N_+\quad N_-$

pulse(0 V_{DD} TD_R TR_R TF_R PW_R PER_R)

and the empirical rules

$$\mathrm{TD}_W + \mathrm{PW}_W \approx \mathrm{TD}_R \qquad (4)$$

$$\mathrm{TR}_R + \mathrm{TF}_R + \mathrm{PW}_R \leq \mathrm{PER}_R \qquad (5)$$

$$\mathrm{TD}_R + \mathrm{PW}_R = \mathrm{PER}_W \qquad (6)$$

$$\mathrm{PER}_R = \frac{\text{time period of the sweeping dc voltage of RTD I-V characteristics}}{N+1 \text{ logic stable states (from } N\text{-peak RTD)}}$$

for CP(W) and CP(R); i.e.,

$V(W)\quad N_+\quad N_-$

pulse (0 7.3 V 0.01 us 0.01 us 0.01 us 9 us 0.019 ms)

$V(R)\quad N_+\quad N_-$

pulse (0 7.3 V 9 us 0.01 us 0.01 us 0.010 ms 0.011 ms)

for nine-state memory circuit simulation, if 0.1 ms is used for the dc voltage sweep period of the eight-peak RTD I-V characteristics. When the write switch S_W controlled by the write pulse $C_P(W)$ is on, the corresponding nine stable states are written into the storage element, (i.e., the combination of eight-peak RTD and MESFET load); and when the read switch S_R is turned on to sense the state of the storage element, the output of the circuit C_{OUT} then gates these nine logic states out of the storage element. The corresponding voltage response waveform of V_{OUT} is obtained through PSpice transient analysis with the simulated results drawn in Fig. 3. One can find that the nine operating point values in Fig. 2 are reproduced with the shape of the nine stable-state waveforms illustrated in Fig. 3. It is noticed that the last two states in the Fig. 3 are somewhat off the operating point values appeared in Fig. 2. This is resulted from an attempt to trade simulation accuracy (iteration limit adjustment in transient analysis) for computation efficiency (CPU times and memory space).

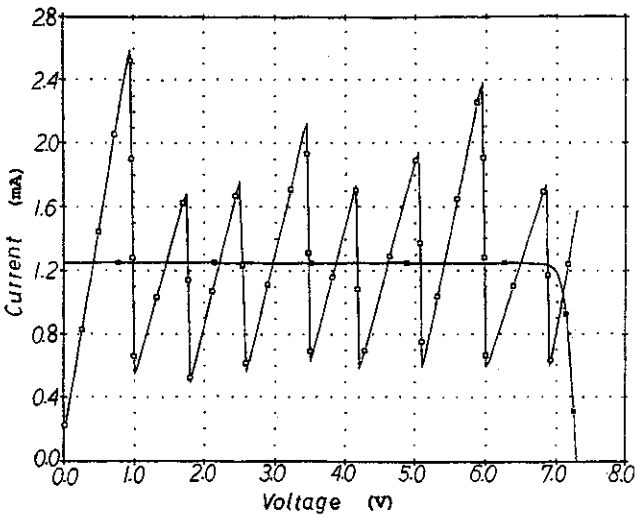

Fig. 2. Simulated eight-peak RTD current-voltage (I-V) characteristics with MESFET depletion-load line.

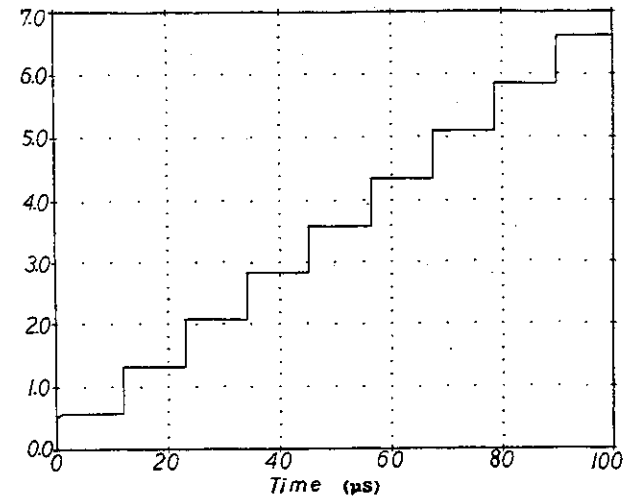

Fig. 3. Simulated results of logic operation waveforms for nine-state RTD-based multivalued memory (MVM) circuit.

III. Conclusion

We have developed an eight-peak RTD piecewise linear (PWL) equivalent circuit model based on an existing multipeak RTD model. The model is successfully implemented into PSpice using the measured voltage and current values of an eight-peak RTD device, and carried out the dc and transient analyses on personal computer for a nine-state MVM circuit simulations.

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